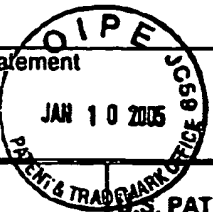


Form PTO-1449 (Modified)		Atty Docket No.: P18612		Serial No.: 10/809,853	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Uday Shah et al.	
				Filing Date: March 24, 2004	



REFERENCE DESIGNATION						
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
<div style="text-align: center;">AC</div> <div style="text-align: center;">AC</div>	AA	6,642,131 B2	Harada 11/2003	438	591	
	AB	6,667,246 B2	Mitsuhashi et al. 12/2003	438	756	
	AC					
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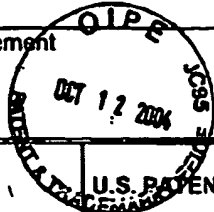
FOREIGN PATENT DOCUMENTS							
No.		Document No.	Date	Country	Class	Sub-Class	Translation
	AQ						
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	AU						

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	AW
	AX
	AY
	AZ

Examiner: <i>Alamp Chaudhary</i>	Date Considered: 5/1/06
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Form PTO-1449 (Modified)	Atty Docket No.: P18612	Serial No.: 10/809,853
List of Patents and Publications Statement (Use several sheets if necessary)	Applicant: Uday Shah	
		Filing Date: March 24, 2004



REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
AC	AA	6,255,698 B1	Gardner et al. 7/2001	257	369	
	AB	6,410,376 B1	Ng et al. 5/2002	438	199	
	AC	6,586,288 B2	Kim et al. 7/2003	438	183	
AC	AD	US 2002/0058374 A1	Kim et al. 5/2002	438	228	
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	AM					
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FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub-Class	Translation
AC	AP	EP 0 899 784 AZ	3/3/1999				
AC	AQ	GB 2 358 737 A	4/24/2001				
	AR						

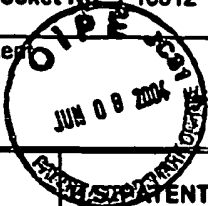
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Examiner: <i>Adams Chambers</i>	Date Considered: 5/1/06
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Form PTO-1449 (Modified)		Atty Docket No. P18612		Serial No.: 10/809,853	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Uday Shah et al.	
				Filing Date: April 20, 2004	



REFERENCE DESIGNATION						
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
AC	AA	6,365,450 B1	Kim 4/2002	438	216	
	AB					
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FOREIGN PATENT DOCUMENTS						
	Document No.	Date	Country	Class	Sub-Class	Translation
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)	
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Examiner: <u>Adam Chomichuk</u>	Date Considered: <u>5/1/06</u>
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Form PTO-1449 (Modified)	Atty Docket No.: P18612	Serial No.: Unknown 10/809, 853
List of Patents and Publications Statement (Use several sheets if necessary)		Applicant: Uday Shah et al.
		Filing Date: March 24, 2004

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS				
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
AC	AA	6,063,698	Tseng et al. 5/2000	438	585	
	AB	6,184,072 B1	Kaushik et al. 2/2001	438	197	
	AC	6,420,279 B1	Ono et al. 7/2002	438	785	
	AD	6,475,874 B2	Xiang et al. 11/2002	438	396	
	AE	6,514,828 B2	Ahn et al. 2/2003	438	240	
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	AG	6,617,209 B1	Chau et al. 9/2003	438	240	
	AH	6,617,210 B1	Chau et al. 9/2003	438	240	
	AI	6,620,713 B2	Arghavani et al. 9/2003	438	585	
	AJ	6,689,675 B1	Parker et al. 2/2004	438	585	
	AK	6,696,327 B1	Brask et al. 2/2004	438	197	
	AL	6,696,345 B2	Chau et al. 2/2004	438	387	
	AM	US2002/0197790 A1	Kizilyalli et al. 12/2002	438	240	
	AN	US2003/0032303 A1	Yu et al. 2/2003	438	770	
AC	AO	US2003/0045080 A1	Visokay et al. 3/2003	438	591	

FOREIGN PATENT DOCUMENTS							
		Document No.	Date	Country	Class	Sub-Class	Translation
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AC	AQ	Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion", www.eesc.berkeley.edu, 1 page
	AR	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages
	AS	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page
	AT	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hamburg-Harburg, 5 pages
	AU	Doczy et al., "Integrating N-type and P-type Metal Gate Transistors," Serial No. 10/327,293, Filed December 20, 2002
	AV	Brask et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode," Serial No. 10/704,497, Filed November 6, 2003
	AW	Brask et al., "A Method for Etching a Thin Metal Layer", Serial No. 10/704,498, Filed November 6, 2003
	AX	Brask et al., "A Method for Making a Semiconductor Device with a Metal Gate Electrode that is Formed on an Annealed High-K Gate Dielectric Layer", Serial No. 10/742,678, Filed 12/19/03
	AY	Brask et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. 10/739,173, filed December 18, 2003
	AZ	Brask et al., "A CMOS Device With Metal and Silicide Gate Electrodes and a Method for Making It", Serial No. 10/748,559, filed December 29, 2003
AC	BA	Doczy et al., "A Method for Making a Semiconductor Device that Includes a Metal Gate Electrode", Serial No. 10/748,545, filed December 29, 2003

Examiner	Andrew Chanilwa	Date Considered	5/1/06
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